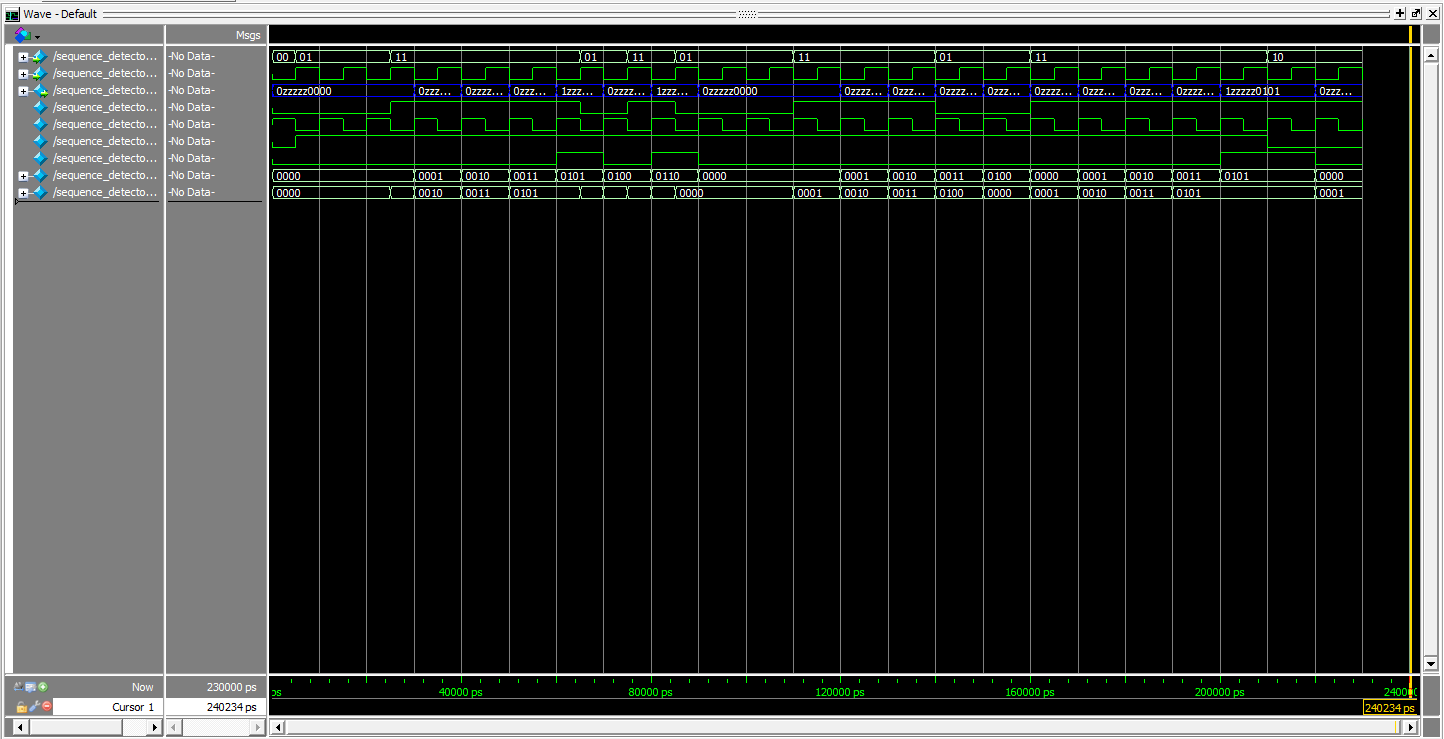
Part I



Clock

Z (LEDR[9])

W (SW[1])

{W, Reset}

Reset (sync)

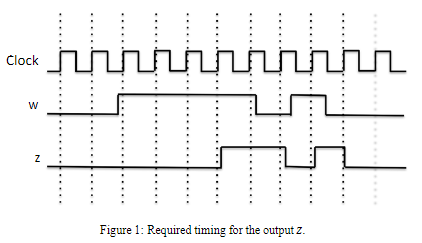
A to F

D to E

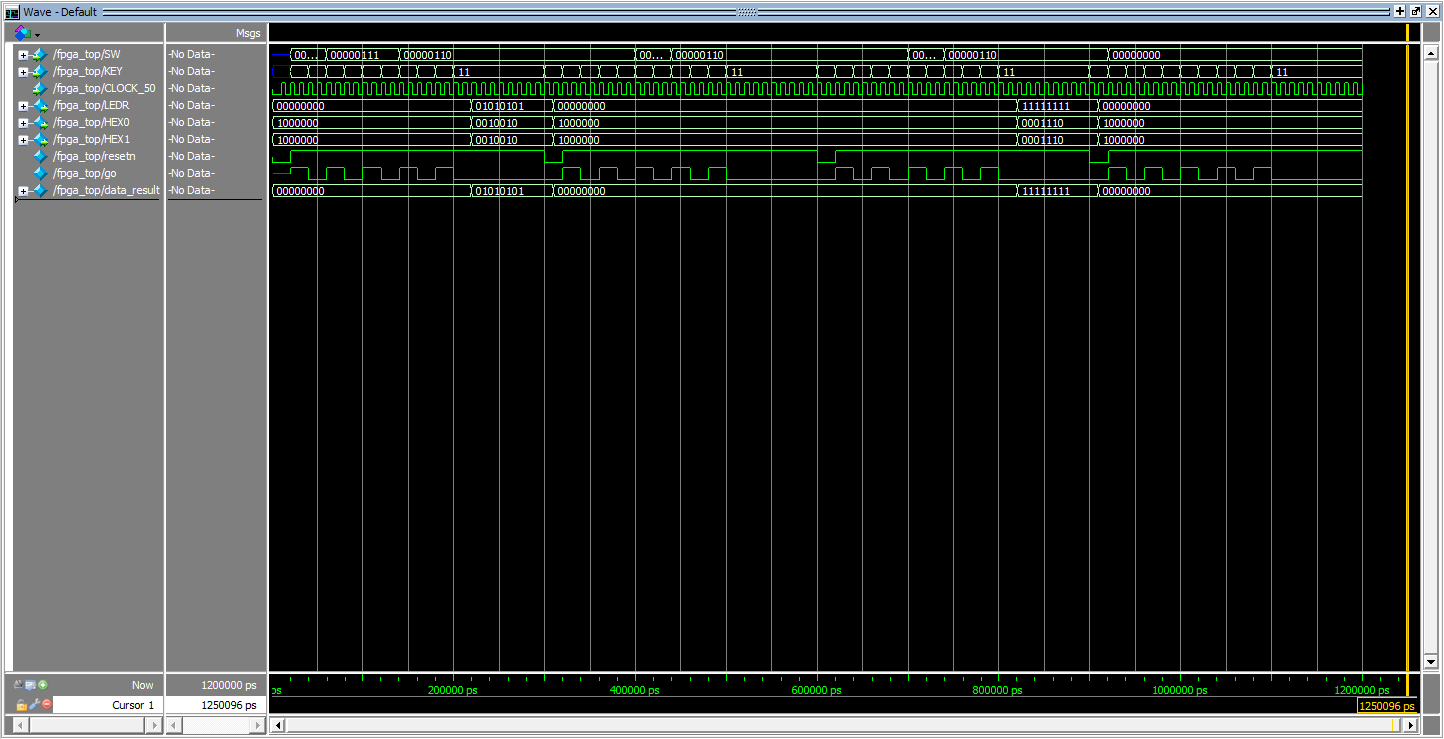
then

E to A

A to D



Part II



Answer

A=0, B=0, C=0, X=0

Ans=0=7’b0

A=6, B=6, C=3, X=6

Ans=255=7’b11111111

A=6, B=6, C=4, X=6

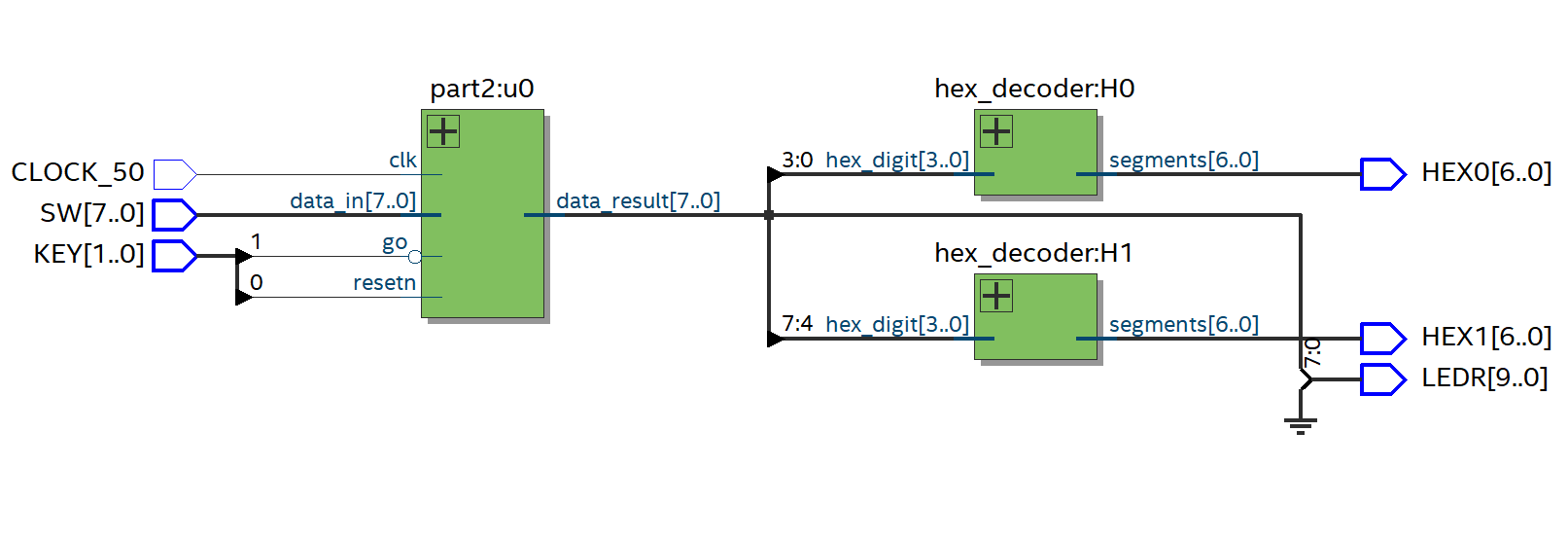
Ans=256=8’b100000000

=7’b0

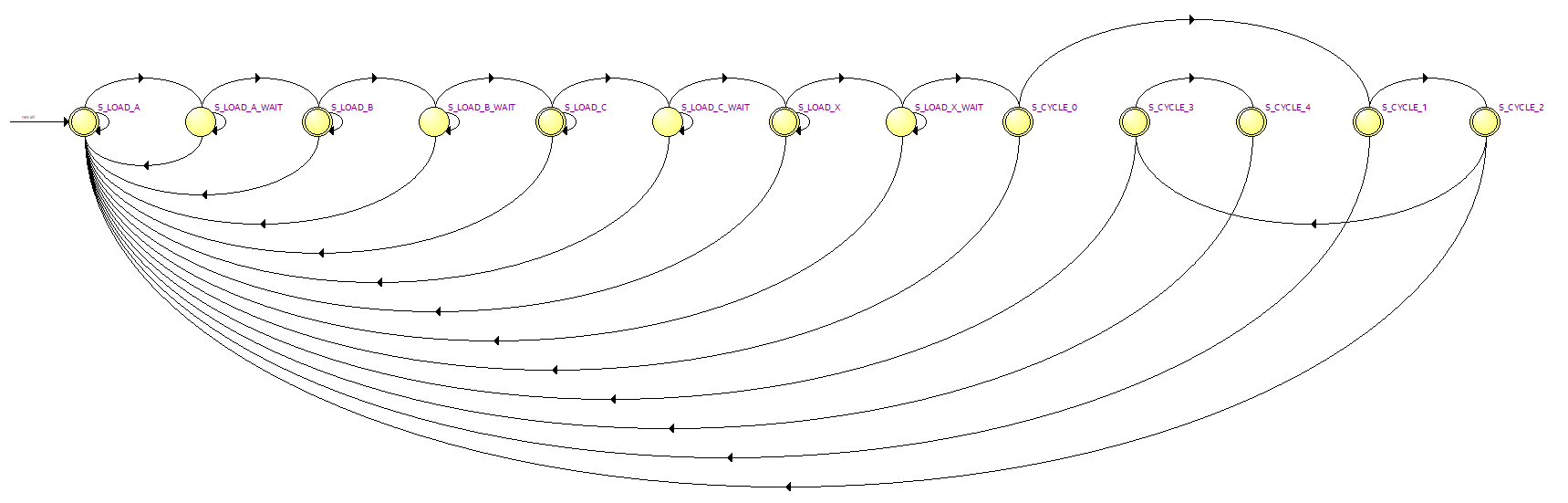
A=1, B=7, C=7, X=6

Ans=85=7’b01010101

RTL Schematic



State Diagram



State Table

|  |  |  |
| --- | --- | --- |
| **Source State** | **Destination State** | **Condition** |
| S\_CYCLE\_0 | S\_CYCLE\_1 | (resetn) |
| S\_CYCLE\_0 | S\_LOAD\_A | (!resetn) |
| S\_CYCLE\_1 | S\_CYCLE\_2 | (resetn) |
| S\_CYCLE\_1 | S\_LOAD\_A | (!resetn) |
| S\_CYCLE\_2 | S\_CYCLE\_3 | (resetn) |
| S\_CYCLE\_2 | S\_LOAD\_A | (!resetn) |
| S\_CYCLE\_3 | S\_CYCLE\_4 | (resetn) |
| S\_CYCLE\_3 | S\_LOAD\_A | (!resetn) |
| S\_CYCLE\_4 | S\_LOAD\_A |  |
| S\_LOAD\_A | S\_LOAD\_A\_WAIT | (go)(resetn) |
| S\_LOAD\_A | S\_LOAD\_A | (!go) + (go)(!resetn) |
| S\_LOAD\_A\_WAIT | S\_LOAD\_B | (!go)(resetn) |
| S\_LOAD\_A\_WAIT | S\_LOAD\_A\_WAIT | (go)(resetn) |
| S\_LOAD\_A\_WAIT | S\_LOAD\_A | (!resetn) |
| S\_LOAD\_B | S\_LOAD\_B\_WAIT | (go)(resetn) |
| S\_LOAD\_B | S\_LOAD\_B | (!go)(resetn) |
| S\_LOAD\_B | S\_LOAD\_A | (!resetn) |
| S\_LOAD\_B\_WAIT | S\_LOAD\_C | (!go)(resetn) |
| S\_LOAD\_B\_WAIT | S\_LOAD\_B\_WAIT | (go)(resetn) |
| S\_LOAD\_B\_WAIT | S\_LOAD\_A | (!resetn) |
| S\_LOAD\_C | S\_LOAD\_C\_WAIT | (go)(resetn) |
| S\_LOAD\_C | S\_LOAD\_C | (!go)(resetn) |
| S\_LOAD\_C | S\_LOAD\_A | (!resetn) |
| S\_LOAD\_C\_WAIT | S\_LOAD\_X | (!go)(resetn) |
| S\_LOAD\_C\_WAIT | S\_LOAD\_C\_WAIT | (go)(resetn) |
| S\_LOAD\_C\_WAIT | S\_LOAD\_A | (!resetn) |
| S\_LOAD\_X | S\_LOAD\_X\_WAIT | (go)(resetn) |
| S\_LOAD\_X | S\_LOAD\_X | (!go)(resetn) |
| S\_LOAD\_X | S\_LOAD\_A | (!resetn) |
| S\_LOAD\_X\_WAIT | S\_LOAD\_X\_WAIT | (go)(resetn) |
| S\_LOAD\_X\_WAIT | S\_CYCLE\_0 | (!go)(resetn) |
| S\_LOAD\_X\_WAIT | S\_LOAD\_A | (!resetn) |